AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Replace paragraph [0029] with the following revised version:

[0029] A variation of this method includes blanket depositing a layer of the conductive material from which the gates are to be formed, and then depositing a layer of resist over the conductive material layer. The resist is patterned according to the desired gate arrangement, and the conductive layer is partially etched to form gate-like structures of the conductive material protruding above the remaining thickness of the conductive material layer. Next, spacers are formed along the sidewalls of the gate-like structures, and the remaining thickness of the conductive layer around the gate-like structures is etched away. During this second etch process, the portion of the conductive material between the spacers is also etched, leaving the resulting gate structures which are spaced apart by approximately the distance between the spacers formed on the sidewalls of adjacent gates.

Replace paragraph [0056] with the following revised version:

[0056] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which ~~is~~ are shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

Replace paragraph [0057] with the following revised version:

[0057] The terms "wafer" and "substrate" used in the description ~~includes~~ include any semiconductor-based structure having an exposed surface on which to form the circuit structure used in the invention. "Wafer" and "substrate" are to be understood as

including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions and/or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but may be based on silicon-germanium, germanium, or gallium arsenide.